**Europäisches Patentamt** 

**European Patent Office** 

Office européen des brevets



EP 0 725 427 A2 (11)

(12)

## **EUROPEAN PATENT APPLICATION**

(43) Date of publication: 07.08.1996 Bulletin 1996/32 (51) Int. Cl.6: H01L 21/00

(21) Application number: 96101602.9

(22) Date of filing: 05.02.1996

(84) Designated Contracting States: BE CH DE ES FR GB IT LI NL SE

(30) Priority: 03.02.1995 US 383112

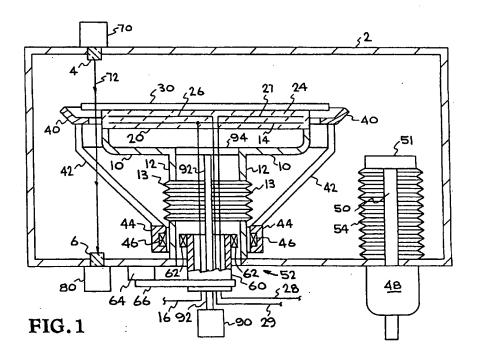
(71) Applicant: Applied Materials, Inc. Santa Clara, CA 95054 (US)

(72) Inventor: Davenport, David E. San Jose, California 95120 (US)

(74) Representative: DIEHL GLAESER HILTL & **PARTNER** Flüggenstrasse 13 80639 München (DE)

## Apparatus and method for semiconductor substrate processing (54)

(57)A semiconductor processing apparatus and process is disclosed which is capable of degassing a semiconductor substrate (30) and also orienting the substrate (30) in the same vacuum chamber (2). The apparatus includes an electrostatic damping structure (10,12,20) for retaining the entire undersurface of a semiconductor substrate (30) in thermal communication therewith in the vacuum chamber (2), a heater (14) located within the electrostatic clamping structure (10,12,20) for heating the electrostatically clamped substrate (30) to degas it, a rotation mechanism (40,42,44) for imparting rotation to the substrate in the vacuum chamber (2), and a detector (80) for detecting the rotational alignment of the substrate (30) in response to the rotation of the substrate (30). In a preferred embodiment, the substrate (30) is rotated to rotationally align it as it is being heated to degas it.



## Description

This invention relates to semiconductor substrate processing.

1

In the processing of semiconductor substrates or wafers in the formation of integrated circuit structures thereon, it is important that the wafer be thoroughly degassed to remove adsorbed gases, moisture, etc. from the wafer prior to, for example, performing a physical vapor deposition (PVD) process to deposit materials on the wafer by sputtering from a target in a vacuum processing chamber. Other processes, such as advanced chemical vapor deposition (CVD) processing, may also require degassing of the wafer. Degassing prior to PVD processing conventionally is carried out at temperatures exceeding 350°C for time periods of from about 40 seconds to about 2 minutes to remove sufficient gases from the wafer to assure a satisfactory deposition by sputtering. Outgassing of substrates during aluminum PVD is more severe than during the prior CVD steps because the PVD process is performed at much higher vacuums and somewhat higher substrate temperatures, both of which induce greater outgassing. Therefore, to avoid outgassing from contaminating the PVD process, the de-gassing of the wafer before the first PVD step must be more extensive than the de-gassing performed before the CVD steps.

Degassing of a wafer is conventionally carried out in one of two ways. One method used to degas a wafer comprises a radiant heating of the wafer, using heat lamps located external to the vacuum chamber containing the wafer, and positioned adjacent transparent windows through which the heat is radiated from the lamps to the wafer. This method is relatively low in cost, is fairly rapid, and does not require clamping of the wafer to the wafer support within the vacuum chamber. However, the radiant heating method is unsatisfactory for temperatures in excess of 350°C, because the temperature of the wafer is not easily controlled, and the heating is usually not uniform across the entire wafer. Typical temperature nonuniformity across the wafer at 350°C is greater than ±30°C. Furthermore, alignment of the rotational orientation of the wafer, during the degassing step, is usually not possible because the radiation from the heat lamps interferes with operation of the optical means conventionally used for such rotational alignment.

The other method conventionally used to degas a wafer, particularly when subsequent PVD processing will be carried out which requires degassing at temperatures in excess of about 350°C, comprises physically (mechanically) clamping the wafer to a wafer support in a vacuum chamber and then heating the wafer using a resistive heater located in the wafer support adjacent the undersurface of the wafer resting on the wafer support. However, since the wafer normally only physically touches the wafer support at the physically clamped periphery or edges of the wafer, and the transmission of heat from the heater in the wafer support to the underside of the wafer via conduction through a vacuum is

very poor, a thermally-conductive gas is normally admitted into the space between the wafer support and the underside of the wafer, with the clamped edge of the wafer serving to at least partially retain the gas in this space. This heating method permits degassification temperatures of as high as about 500-600°C to be achieved.

This method thus permits the use of degassing temperatures in excess of 350°C, and permits measurement and reasonable control of the temperature of the wafer. However, alignment of the rotational orientation usually cannot be carried out during the degassing step because the conduit for the thermally conductive gas inhibits rotation of the chuck. The clamping ring also inhibits rotation due to its weight. Rotation of a clamped wafer could also cause wafer breakage and particles. The alignment of the rotational orientation of the wafer must, therefore, be carried out in a separate chamber prior to the degassing step. Furthermore, because this form of degassing must be preformed in a chamber very similar to a PVD chamber (i.e., it must include a cryopump, heated chuck, wafer lift assembly, cryo isolation valve, transfer chamber, isolation valve, clamp ring, etc.), it is a very expensive solution. Also typical temperature uniformities across the wafer achieved with this type of degassing apparatus are approximately ±10 to 15°C. Temperature uniformities of ±5°C are required for advanced devices.

Furthermore, regardless of which heating method is used, because of the extended time period needed for degassing prior to PVD processing, the degassing step can reduce process throughput. One prior art approach which has been considered for solving this particular problem is to provide parallel degassing chambers, i.e., two degassing chambers are provided in a semiconductor wafer processing apparatus for each PVD processing chamber. However, this adds considerable extra cost to the apparatus. In addition, when the rotational orientation of the wafer must also be carried out in a separate chamber, either three or four preprocessing chambers must be untilized (depending whether or not each of the two parallel degassing chamber is coupled to its own separate rotational orientation chamber), which greatly adds to the overall expense of the apparatus.

It would, therefore, be desirable to be able to consolidate the rotational alignment and degassing of the wafer into a single chamber which would avoid the expense of separate chambers, as well as the additional time consumed during transfer of the wafer from one chamber to the other. It would be of further advantage if the degassing could be carried out at high temperatures, i.e., temperatures in excess of about 350°C, without mechanically clamping the wafer to the wafer support, and while still maintaining an even and controllable heating of the wafer. It would be even more advantageous if both the degassing and the rotational orientation of the wafer could be carried out simultaneously in the same chamber at a high temperature and

without mechanical clamping the wafer to the wafer support.

This desire is fulfilled by the provision of a semiconductor processing apparatus according to independent claim 1 and a process according to independent claim 14.

Further advantageous features, aspects, and details of the invention are evident from the dependent claims, the description and the drawings. The claims are intended to be understood as a first non-limiting approach of defining the invention in general terms.

More particularly, this invention relates to apparatus and method for rotationally aligning and degassing a semiconductor substrate in the same vacuum chamber.

In accordance with the invention, a semiconductor processing system is provided which is capable of degassing a semiconductor substrate at temperatures as high as 500°C and preferably also rotationally aligning the substrate in the same vacuum chamber, without the use of a mechanical clamping ring and thermally conductive gas. The apparatus of the semiconductor processing system includes a heated electrostatic clamping structure for supporting the semiconductor wafer and retaining the substrate in thermal communication therewith in the vacuum chamber, a heater within the electrostatic clamping structure for heating the electrostatically clamped substrate to degas it, a rotation mechanism for imparting rotation to the substrate in the same vacuum chamber, and a detector for detecting the rotational alignment of the substrate in the vacuum chamber in response to the rotation of the substrate. Preferably, the entire undersurface of the semiconductor substrate is retained in thermal communication. In a preferred embodiment, the substrate is rotated to rotationally align it as it is being heated to degas it without, however, using mechanical clamping apparatus to secure the substrate to a substrate support. In an alternate embodiment, the substrate may be rotated for alignment either prior to or after degassification, but in the same chamber.

Further features and advantages of this invention will become more readily apparent from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figure 1 is a vertical cross-sectional view in schematic form of a degasification and rotational alignment chamber of a semiconductor substrate processing apparatus comprising one embodiment of the invention wherein the substrate is rotationally aligned using a lift ring within the vacuum chamber to rotate the substrate.

Figure 2 is an isometric view illustrating the optical orientation apparatus shown in Figure 1 for rotationally aligning the substrate.

Figure 3 is a vertical cross-sectional view in schematic form of a degasification and rotational alignment chamber of a semiconductor substrate processing apparatus comprising another embodiment of the invention wherein the substrate is rotationally aligned by rotation of the substrate support and electrostatic chuck therein.

The invention comprises a semiconductor processing system capable of degassing a semiconductor substrate or wafer at temperatures as high as 500°C or higher, depending upon the temperature sensitivity of other materials already on the wafer, and also capable of aligning the rotational orientation of the wafer in the same vacuum chamber, without the use of a mechanical clamping ring and thermally conductive gas. The system utilizes an electrostatic clamping means for retaining the semiconductor wafer in thermal communication with a wafer support in the vacuum chamber while the wafer is heated by a heater within the wafer support to degas it. A rotation mechanism for imparting rotation to the wafer in the vacuum chamber and a detector for detecting the rotational alignment of the wafer in response to the rotation of the wafer are also provided. In a preferred embodiment, the wafer is simultaneously rotated to rotationally align it while it is being heated to degas it.

Turning now to Figure 1, one embodiment of the system of the invention is generally illustrated wherein a vacuum chamber 2 is provided with a wafer support 10, which may comprise a stainless steel material, mounted on a pedestal 12. Forming the top surface of wafer support 10 is an electrostatic clamping means or chuck 20 which, in the illustrated embodiment, comprises an insulative material 24, such as aluminum oxide, aluminum nitride, or other ceramic material, on the top surface of wafer support 10 and having embedded therein metallic electrodes 26 and 27 which are connected through leads 28 and 29 to a high voltage source (not shown) external to vacuum chamber 2. Also embedded within chuck 20 is a heater 14, such as a resistance heater, which may be connected through lead(s) 16 to a power source (not shown) external to vacuum chamber 2. The inside of wafer support 10 and pedestal 12 are at atmospheric pressure. Wafer support 10 is brazed to ceramic chuck 20 to provide a vacuum seal.

A wafer 30, to be degassed and rotationally aligned, may be placed on electrostatic chuck 20 and electrodes 26 and 27 energized with a high voltage, e.g., about 500-5000 volts DC, to thereby electrostatically clamp wafer 30 to the surface of electrostatic chuck 20. Wafer 30 is removed from the system transfer robot (not shown) for placement on electrostatic chuck 20 (and later removals by lift pins or fingers (not shown) on a ring (also not shown) attached to support plate 51 which, in turn, is connected to a pneumatic or motor-driven lift motor 48 and shaft 50 through a vacuum isolation bellows 54.

Heater 14 is energized to thereby heat electrostatic chuck 20 which then heats wafer 30 through direct conduction. It should be noted that unlike prior art secure-

45

ment of the wafer to an upper surface of a wafer support during the heating of the wafer, not only is the periphery of the wafer in thermal contact with electrostatic chuck 20 (to provide thermal coupling therebetween), but all of the undersurface of wafer 30 is also in mechanical contact with electrostatic chuck 20 and therefore thermally coupled to electrostatic chuck 20 due to the uniformity of the electrostatic forces across the surface of electrostatic chuck 20. Heater 10 advantageously is activated prior to the electrostatic clamping of wafer 30 to electrostatic chuck 20 to preheat electrostatic chuck 20 and thereby accelerate the heating process. Because of the intimate contact of the wafer to the heated electrostatic chuck, gas between the wafer and the chuck is not required.

Wafer 30 is also rotationally aligned in vacuum chamber 2. Alignment of the rotational or angular orientation of a semiconductor wafer is necessary to provide the correct rotational alignment of a semiconductor wafer in a processing chamber, as is well known to those skilled in the art. Such rotational alignment is facilitated by the provision of some sort of alignment indicia on the wafer itself. A common alignment means is the provision of a flat or notch on one portion of the circumference of a normally circular wafer. A beam of light from a light source is then usually directed perpendicular to the plane of the wafer to intercept the wafer adjacent its edge. As the wafer is rotated, the light is reflected back to the source until the flat or notched portion is encountered, at which point the light beam is transmitted to a photo detector positioned on the other side of the wafer.

As shown in Figure 1, a ring 40 may be provided to rotate wafer 30 to rotationally align wafer 30 in vacuum chamber 2. When it is desired to rotate wafer 30, the wafer is lowered onto rotatable ring 40. Wafer 30 is lowered onto ring 40 by activation of fluid powered motor 90 to which is attached a shaft 92, as shown in Figure 1, which is centrally mounted within pedestal 12. Shaft 92 is coupled to the upper portion of pedestal 12 by a cross bar 94. Bellows 13 on pedestal 12 permit the upper portion of pedestal 12, with support 10 and electrostatic chuck 20 secured thereto, to move up and down (vertically) while maintaining the vacuum within chamber 2. This, in turn, permits the desired lowering of wafer 30 onto rotatable ring 40, and subsequent raising of wafer 30 off ring 40 when the orientation step is complete.

Ring 40 is provided with arms 42 which are, in turn, connected to a central cylinder 44 to which are attached a first set of magnets 46 which form a part of magnetic coupling mechanism 52. A hollow shaft 60 located within pedestal 12 has a second set of magnets 62 mounted thereon forming the other portion of magnetic coupling mechanism 52. A motor 64 rotates shaft 60 via a belt 66 and this rotation is transmitted through magnetic coupling mechanism 52 to cylinder 44 and ring 40 to thereby rotate wafer 30.

As wafer 30 is rotated on ring 40 by motor 64, a light source 70, external to vacuum chamber 2, directs a light beam 72 through a first window 4 in the top wall of vacuum chamber 2 toward the top surface of wafer 30 adjacent the periphery thereof. When flat portion or notch 32 of wafer 30 is encountered, as shown in Figure 2, light beam 72 passes through to a second window 6 located in the bottom wall of vacuum chamber 2 and is detected by photodetector 80, signifying the rotational position of the flat or notched portion 32 of wafer 30.

In the embodiment shown in Figures 1 and 2, the rotational alignment of wafer 30 is carried out in the same vacuum chamber as the degassification of wafer 30. However, the rotational alignment and degassification are carried out sequentially, rather than simultaneously. The rotational alignment may be carried out either before or after the degassifying of wafer 30.

It would, however, be even more advantageous if, in addition to using the same vacuum chamber for both rotational orientation and degassifying of the wafer, both steps could be carried out simultaneously. Figure 3 illustrates another embodiment of the invention which permits such simultaneous rotational orientation and degassifying of a semiconductor wafer by rotating the wafer support and electrostatic chuck with the wafer clamped thereto so that the wafer continues to be heated and therefore degassified while the rotational orientation of the wafer is carried out by the light source and photodetector.

In Figure 3, wherein like elements are identified with like numerals, the pedestal beneath wafer support 10 comprises a hollow cylinder 112 with its cylindrical wall magnetically coupled through magnetic coupling mechanism or clutch 152 to a hollow cylindrical shaft 160 external to vacuum chamber 2. Cylindrical shaft 160 is, in turn, connected to a motor 164 which rotates cylindrical shaft 160 and this rotation is transmitted through magnetic coupling 152 to cylindrical pedestal 112 to thereby rotate wafer support 10, electrostatic chuck 20, and wafer 30 clamped thereto.

A flexible heater lead 116 connects heater lead 16 within vacuum chamber 2 to an external heater lead 118; while flexible high voltage leads 128 and 129 connect high voltage leads 28 and 29 with external high voltage lead 138 and 139. This provision of such flexible leads permits rotation of wafer support 10, for example, 180° in each direction while still maintaining electrical contact respectively to heater 14 and electrostatic chuck electrodes 26 and 27.

As described in the previous embodiment, as wafer 30 is rotated by motor 164, light source 70, external to vacuum chamber 2, directs light beam 72 through first window 4 in the top wall of vacuum chamber 2 toward the top surface of wafer 30 adjacent the periphery thereof. When flat portion 32 of wafer 30 is encountered, as previously shown and described in Figure 2, light beam 72 passes to and through second window 6 located in the bottom wall of vacuum chamber 2 and is detected by photodetector 80, signifying the rotational position of flat or notched portion 32 of wafer 30.

Thus the semiconductor wafer processing system of the invention permits degassifying and rotational

20

25

alignment of a semiconductor wafer to be carried out in the same vacuum chamber with temperatures above 350°C being utilizable without, however, mechanical clamping the wafer to the wafer support. In a preferred embodiment, rotational alignment and degassification 5 of the semiconductor wafer may be carried out simultaneously in the same chamber.

## Claims

- 1. Semiconductor processing apparatus, comprising:
  - a. a vacuum chamber (2);
  - structure 15 (10,12,20,112) functioning as a substrate support for retaining a semiconductor substrate (30) in thermal communication therewith in said
  - trostatically clamped substrate (30) to degas said substrate (30).
- 2. The semiconductor processing apparatus of claim substrate (30) in said vacuum chamber (2); and tion of said substrate (30).
- 3. The semiconductor processing apparatus of claim (10,12,20,112) is a heated electrostatic clamping structure (10, 12, 20, 112).
- substrate support in thermal communication with said substrate (30).
- 5. The semiconductor processing apparatus of any of surface thereof facing an undersurface of said substrate, and one or more high voltage electrodes (26,27) in said insulation.
- the preceding claims wherein said electrostatic clamping structure comprises one high voltage 55 electrode (26,27) in said insulation.

(40,42,44,60,112,160) comprise a rotatable ring (40) within said vacuum chamber (2).

- 8. The semiconductor processing apparatus of claim 7, wherein said rotatable ring is capable of lifting said substrate off said substrate support.
- The semiconductor processing apparatus of any of claims 2 to 8 wherein said rotation mechanism (40,42,44,60,112,160) further comprise a magnetic coupling (46,62) to couple said rotating ring (40) to a source of rotation (60,64,66,160,166) outside of said vacuum chamber (2).
- 10. The semiconductor processing apparatus of any of claims 2 to 9 wherein said rotation mechanism (40,42,44,60,112,160) comprises a rotatable electrostatic clamping mechanism (20) to permit said substrate to be rotationally aligned while said substrate (30) is heated to degas said substrate (30).
- 11. The semiconductor processing apparatus of any of the preceding claims wherein said electrostatic clamping structure (10,12,20,112) comprises an electrostatic clamping mechanism on a substrate support, said electrostatic clamping mechanism comprising insulation on the surface of said substrate support facing an undersurface of said substrate, and a high voltage electrode in said insulation:
  - a heater within said electrostatic clamping mechanism for heating said electrostatically clamped substrate to degas said substrate.
- 12. The semiconductor processing apparatus of any of the preceding claims, wherein said substrate (30) is a wafer.
  - 13. The semiconductor processing apparatus of any of the preceding claims whereby said semiconductor wafer can be rotationally aligned while being simultaneously heated to degasify said wafer.
  - 14. A process for degassing a semiconductor substrate which comprises:
    - a) providing a vacuum chamber (2);
    - b) retaining a semiconductor substrate (30) in thermal communication with an electrostatic clamping structure (10, 12,20,112) in said vacuum chamber (2);
    - c) heating said substrate (30) to degas said electrostatically clamped substrate (30) by providing a heater (14) within said electrostatic clamping structure (10,12,20,112).

5

b. an electrostatic clamping

vacuum chamber (2);

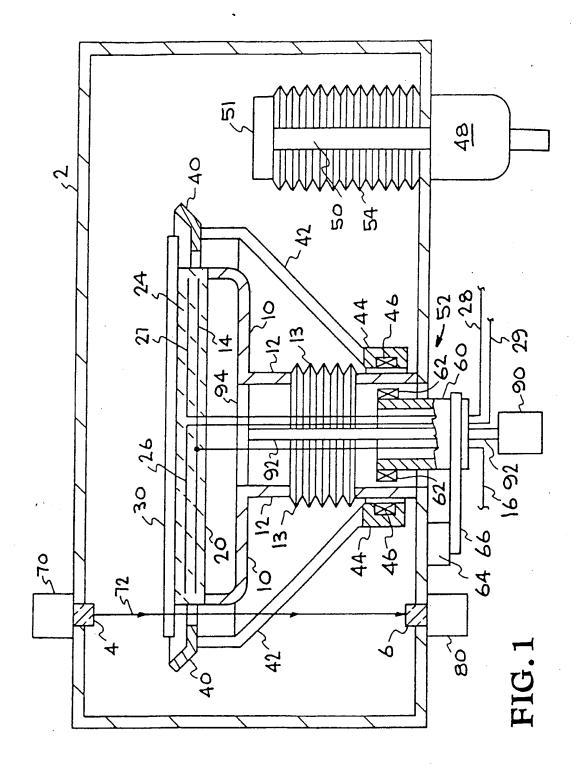
- c. a heater (14) within said electrostatic clamping structure (10,12,20) for heating said elec-
- 1. further comprising a rotation mechanism (40,42,44,60,112,160) for imparting rotation to said a detector (80) for detecting the rotational alignment of said substrate (30) in response to said rota-
- 1 or 2, wherein said electrostatic clamping structure
- 4. The semiconductor processing apparatus of any of the preceding claims wherein said heater (14) comprises a resistance heater (14) in said electrostatic clamping structure (20) adjacent a surface of said
- the preceding claims wherein said electrostatic clamping structure (20) comprises insulation on the
- 6. The semiconductor processing apparatus of any of
- 7. The semiconductor processing apparatus of any of claims 2 to 6 wherein said rotation mechanism

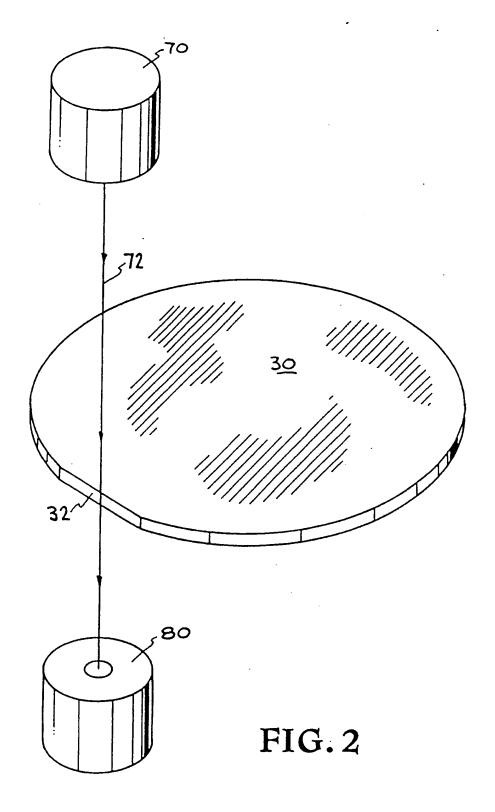
40

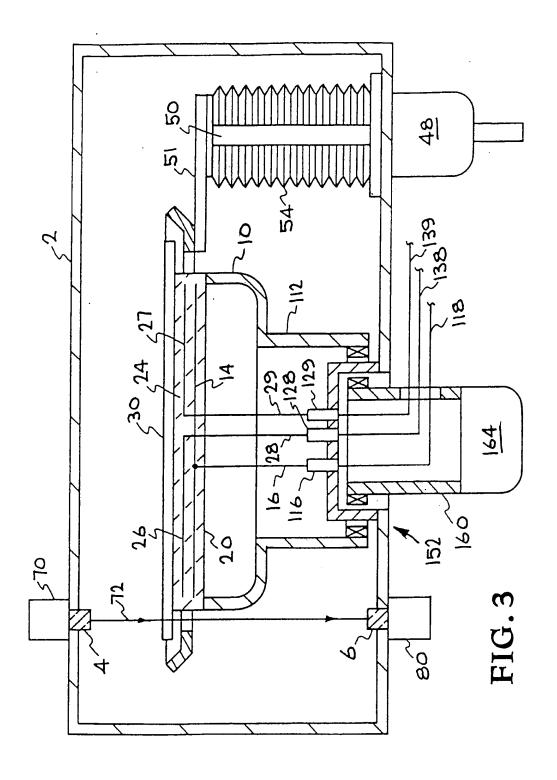
45

50

- 15. The process of claim 14 further comprising rotating said substrate (30) in said vacuum chamber (2); and detecting the rotational alignment of said substrate in response to said rotating of said substrate
- 16. The process of claim 14 or 15 wherein said step of heating said substrate (30) further comprises providing a resistance heater (14) in said electrostatic clamping structure (10,12,20,112) adjacent a sur- 10 face thereof in thermal communication with said substrate (30).
- 17. The process of any of claims 14 to 16 wherein said electrostatic clamping structure (10,12,20,112) 15 comprises insulation on the surface thereof facing an undersurface of said substrate (30), and a high voltage electrode in said insulation.
- 18. The process of any of claims 14 to 17 wherein said 20 step of rotating said substrate (30) further comprises magnetically coupling a rotatable ring (40) used for rotating said substrate (30) to a source of rotation (60,64,66,160,164) outside of said vacuum chamber.
- 19. The process of any of claims 14 to 18 wherein said step of rotating said substrate further comprises lifting said substrate (30) off said substrate support (20) using said rotatable ring (40) within said vac- 30 uum chamber (2).
- 20. The process of any of claims 14 to 18 wherein said step of rotating said substrate further comprises rotating said electrostatic clamping structure 35 (10,12,20,112) to permit said step of detecting the rotational alignment of said substrate (30) to be carried out during said heating step to degas said substrate (30).







THIS PAGE BLANK (USPTO)